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EXAMINER	
CLEARY, THOMAS J	

ART UNIT	PAPER NUMBER
2181	7

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/751,449	HEITKAMP ET AL.	
	Examiner	Art Unit	
	Thomas J. Cleary	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 October 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22,24 and 25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *20 and 21* is/are allowed.

6)☒ Claim(s) *1-19,22,24 and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 103

2. Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Number 6,526,464 to Jobs et al. ("Jobs") in view of US Patent Number 6,381,239 to Atkinson et al. ("Atkinson") and US Patent Number 6,273,771 to Buckley et al. ("Buckley").

In reference to Claim 1, Jobs teaches a master control processor (See Figure 2 Number 240); a bus controller connected to the processor that implements a serial bus interface between the processor and a plurality of serial bus devices (See Figure 2 Number 202); and a switch configured to electrically connect the circuit board corresponding to the switch to the first circuit board through the serial bus interface when the switch is controlled to be in a first state and to electrically isolate the circuit board corresponding to the switch from the serial bus interface on the first circuit board when the switch is controlled to be in a second state (See Figure 2 Numbers 206 and 208). Jobs does not teach the processor and bus controller being on a first circuit board; a midplane connected to the bus controller on the first circuit board; a plurality of additional circuit boards connected to the serial bus interface through the midplane;

each additional board including one or more of the serial bus devices; local control logic for outputting a signal for controlling the state of the switch; and the local control logic controlling the switch to be in the first state when the switches on each of the other of the plurality of additional circuit boards are in the second state. Atkinson teaches a midplane which has a plurality of cards connected to it (See Figure 1 Number 1, and Column 9 Lines 12-15); a serial message bus connecting the cards across the midplane (See Figure 1 Number 9); and a processor and bus interface on a first circuit board (See Figure 1 Numbers 44, 46, and 48). Buckley teaches a local control logic connected to a valve (analogous to the switch) and controlled by a control processor (See Figure 4, Column 18 Lines 64-67, and Column 19 Lines 1-20).

In reference to Claim 2, Jobs, Atkinson, and Buckley teach the limitations as applied to Claim 1 above. Jobs further teaches basic input-output routines in NVRAM (analogous to the master control logic) connected to the master control processor to control the gates (See Figure 2 Number 228 and Column 2 Lines 46-49). Buckley further teaches that the local control logic for the valve-switch is controlled by a master controller (analogous to master control logic) (See Figure 4 and Column 18 Lines 64-67 and Column 19 Lines 1-9).

One of ordinary skill in the art at the time the invention was made would combine the devices of Jobs, Atkinson, and Buckley, resulting in the invention of Claims 1 and 2, in order to provide a means for allowing system expandability (See Column 6 Lines 6-10 of Atkinson); increased flexibility (See Column 6 Lines 11-14 of Atkinson); a dense package (See Column 8 Lines 62-63 of Atkinson); and to convert the signal compatible

with the bus protocol to a signal appropriate for controlling the valve switch (See Column 18 Lines 66-67 and Column 19 Lines 1-6 of Buckley).

3. Claims 3 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jobs, Atkinson, and Buckley as applied to Claim 2 above, and further in view of US Patent Number 6,301,623 to Simpson et al. ("Simpson").

In reference to Claim 3, Jobs, Atkinson, and Buckley teach the limitations as in Claim 2 above. Jobs, Atkinson, and Buckley do not teach a multiplexer connected to the output of the bus controller and dividing the serial bus interface into a plurality of sub-buses, only one of which is connected to the bus controller by the multiplexer at any given time. Simpson teaches the use of a multiplexer to divide a serial channel into a plurality of device groups, only one of which is accessible at a time (See Abstract, Figure 4, Column 1, Lines 66-67, and Column 2, Lines 1-15 of Simpson).

In reference to Claim 6, Jobs, Atkinson, Buckley, and Simpson teach the limitations as in Claim 3 above. Jobs, Atkinson, and Buckley do not teach one of the sub-buses being connected to the plurality of additional circuit boards Simpson further teaches that a plurality of stations (analogous to the circuit boards) can be connected to each sub-bus through the communication module (See Figure 2 and Column 3 Lines 60-67).

One of ordinary skill in the art at the time the invention was made would combine the device of Jobs, Atkinson, and Buckley with the device of Simpson, resulting in the

inventions of Claims 3 and 6, in order to allow virtually limitless expansion of the address space (See Column 2, Lines 58-63 of Simpson).

4. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jobs, Atkinson, Buckley, and Simpson as applied to Claim 3 above, and further in view of US Patent Number 6,532,500 to Li et al. ("Li") and US Patent Number 6,122,756 to Baxter et al. ("Baxter").

In reference to Claim 4, Jobs, Atkinson, Buckley, and Simpson teach the limitations as in Claim 3 above. Jobs, Atkinson, Buckley, and Simpson do not teach the serial bus devices including at least one of a temperature sensor, a voltage monitor, and an ID EPROM. Li teaches a serial temperature sensor and a serial voltage sensor (See Column 4 Lines 23-49 of Li). Baxter teaches an ID EPROM device (See Figure 2 Number 204).

In reference to Claim 5, Jobs, Atkinson, Buckley, and Simpson teach the limitations as in Claim 3 above. Jobs, Atkinson, Buckley, and Simpson do not teach one of the serial bus devices including an ID EPROM connected to the midplane. Baxter teaches a system ID SEEPROM (Serial EEPROM) device located on the backpanel (analogous to the midplane) (See Column 10 Lines 27-29).

One of ordinary skill in the art at the time the invention was made would combine the device of Jobs, Atkinson, Buckley, and Simpson, with the devices of Li and Baxter, resulting in the inventions of Claims 4 and 5, in order to provide signals representing the operating parameters of various devices in the computer system such as temperature

and voltage (See Column 4 Lines 23-26 and Column 4 Lines 30-33 of Li); and provide a non-volatile way to store important system information (See Column 11 Lines 42-44 of Baxter).

5. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jobs, Atkinson, and Buckley as applied to Claim 1 above, and further in view of US Patent Number 4,845,736 to Posner et al. ("Posner").

In reference to Claim 7, Jobs, Atkinson, and Buckley teach the limitations as in to Claim 1 above. Jobs, Atkinson, and Buckley do not teach a first switch for selectively connecting or disconnecting a first portion of a serial bus, implemented by the serial bus interface from the first circuit board, to a second portion of the serial bus; a second switch for selectively connecting or disconnecting the second portion of the serial bus to a third portion of the serial bus; and a third switch for selectively connecting or disconnecting the third portion of the serial bus to a fourth portion of the serial bus. Posner teaches a plurality of cross connect switches that can have any number of inputs and outputs (See Figure 11 and Column 1 Lines 38-41); wherein the input (analogous to the first bus portion) is connected to the first switch, the first switch has a connection to the second switch (analogous to the second bus portion), the second switch has a connection to the third switch (analogous to the third bus portion), and the third switch is connected to the output (analogous to the fourth bus portion) (See Figure 11).

In reference to Claim 8, Jobs, Atkinson, Buckley, and Posner teach the limitations as in Claim 7 above. Atkinson further teaches an application processor (analogous to the local processor) connected to the serial bus through a communication processor (analogous to the bus controller) (See Figure 1 Numbers 9, 12, and 16). Posner further teaches a computer (analogous to the local control logic) that is used to control the first, second, and third switches (See Figure 11 Number 422 and Column 15 Lines 33-34).

One of ordinary skill in the art at the time the invention was made would combine the device of Jobs, Atkinson, and Buckley with the device of Posner, resulting in the invention of Claims 7 and 8, in order to provide a means of testing the connections between the first portion of the bus and the fourth portion of the bus (See Column 15 Lines 12-19 of Posner); and to reduce the capacitive loading of the devices on the bus by disconnecting segments not in use, since it is known in the art that capacitive loading degrades performance.

6. Claims 9, 10, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jobs in view of Atkinson and US Patent Number 6,330,614 to Aggarwal et al. ("Aggarwal").

In reference to Claim 9, Jobs teaches a device (analogous to the packet forwarding engine) comprising a first circuit board having a master control processor (See Figure 2 Number 240); and a plurality of switches configured to electrically connect a serial bus to the first circuit board when the switch is controlled to be in a first state

and to electrically isolate the serial bus from the first circuit board when the switch is controlled to be in a second state, wherein the switch of a particular serial bus being in the first state only when the switches for each of the other serial busses are in the second state (See Figure 2 Numbers 206 and 208 and Column 2 Lines 26-39). Jobs does not teach a routing engine for consolidating routing information learned from routing protocols in the network; the packet forwarding engine including a midplane; and a plurality of second circuit boards each having a control processor. Aggarwal teaches a routing engine (See Figures 3 and 4, Column 4, Lines 34-38, and Column 5, Lines 49-66 of Aggarwal). Atkinson teaches a midplane which has a plurality of cards connected to it (See Figure 1 Number 1, and Column 9 Lines 12-15); a serial message bus connecting the cards across the midplane (See Figure 1 Number 9); a processor and bus interface on a first circuit board (See Figure 1 Numbers 44, 46, and 48); and a control processor on each of the second circuit boards (See Figure 1 Number 12).

In reference to Claim 10, Jobs, Atkinson, and Aggarwal teach the limitations as in Claim 9 above. Aggarwal further teaches that the network device is a network router (See Figures 3 and 4, Column 2 Lines 26-42, and Column 5, Lines 49-66).

In reference to Claim 13, Jobs, Atkinson, and Aggarwal teach the limitations as applied to Claim 9 above. Jobs further teaches a bus controller connected to the processor that implements a serial bus interface between the processor and a plurality of serial bus devices (See Figure 2 Number 202).

One of ordinary skill in the art at the time the invention was made would combine the devices of Jobs, Atkinson, Buckley, and Aggarwal, resulting in the invention of

Claims 9, 10, and 13, in order to provide a means for allowing system expandability (See Column 6 Lines 6-10 of Atkinson); increased flexibility (See Column 6 Lines 11-14 of Atkinson); a dense package (See Column 8 Lines 62-63 of Atkinson); to convert the signal compatible with the bus protocol to a signal appropriate for controlling the valve switch (See Column 18 Lines 66-67 and Column 19 Lines 1-6 of Buckley); and to create a forwarding table allowing the device to determine the proper output port based on the destination address of incoming packets (See Column 6 Lines 4-48 of Aggarwal).

7. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jobs, Atkinson, and Aggarwal as applied to Claim 9 above, and further in view of Buckley.

In reference to Claim 11, Jobs, Atkinson, and Aggarwal teach the limitations as in Claim 9 above. Jobs, Atkinson, and Aggarwal do not teach local control logic coupled to receive control information from the master control processor and the control processor corresponding to the second circuit board of the local control logic; and the local control logic controlling the switch to be in the first or second state based on the received control information. Buckley teaches a local control logic connected to a valve (analogous to the switch) and controlled by either a master control processor (See Figure 4, Column 18 Lines 64-67, and Column 19 Lines 1-20) or another device on the bus (analogous to the local control processor) (See Column 19 Lines 52-65).

In reference to Claim 12, Jobs, Atkinson, Aggarwal, and Buckley teach the limitations as applied to Claim 11 above. Jobs further teaches basic input-output

routines in NVRAM (analogous to the master control logic) connected to the master control processor to control the gates (See Figure 2 Number 228 and Column 2 Lines 46-49). Buckley further teaches that the local control logic for the valve-switch is controlled by a master controller (analogous to master control logic) (See Figure 4 and Column 18 Lines 64-67 and Column 19 Lines 1-9).

One of ordinary skill in the art at the time the invention was made would combine the device of Jobs, Atkinson, and Aggarwal with the device of Buckley, resulting in the invention of Claims 11 and 12, in order to convert the signal compatible with the bus protocol to a signal appropriate for controlling the valve switch (See Column 18 Lines 66-67 and Column 19 Lines 1-6 of Buckley).

8. Claims 14 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jobs, Atkinson, and Aggarwal as applied to Claim 13 above, and further in view of Simpson.

In reference to Claim 14, Jobs, Atkinson, and Aggarwal teach the limitations as in Claim 13 above. Jobs, Atkinson, and Aggarwal do not teach a multiplexer connected to the output of the bus controller and dividing the serial bus interface into a plurality of sub-buses, only one of which is connected to the bus controller by the multiplexer at any given time. Simpson teaches the use of a multiplexer to divide a serial channel into a plurality of device groups, only one of which is accessible at a time (See Abstract, Figure 4, Column 1, Lines 66-67, and Column 2, Lines 1-15 of Simpson).

In reference to Claim 17, Jobs, Atkinson, Aggarwal, and Simpson teach the limits as applied to Claim 14 above. Atkinson further teaches a serial bus that is connected to a plurality of circuit boards (See Figure 1 Number 9).

One of ordinary skill in the art at the time the invention was made would combine the device of Jobs, Atkinson, and Aggarwal with the device of Simpson, resulting in the inventions of Claims 14 and 17, in order to allow virtually limitless expansion of the address space (See Column 2, Lines 58-63 of Simpson).

9. Claims 15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jobs, Atkinson, Aggarwal, and Simpson as applied to Claim 14 above, and further in view of Li and Baxter.

In reference to Claim 15, Jobs, Atkinson, Aggarwal, and Simpson teach the limitations as in Claim 14 above. Jobs, Atkinson, Aggarwal, and Simpson do not teach the serial bus devices including at least one of a temperature sensor, a voltage monitor, and an ID EPROM. Li teaches a serial temperature sensor and a serial voltage sensor (See Column 4 Lines 23-49 of Li). Baxter teaches an ID EPROM device (See Figure 2 Number 204).

In reference to Claim 16, Jobs, Atkinson, Aggarwal, and Simpson teach the limitations as in Claim 14 above. Jobs, Atkinson, Aggarwal, and Simpson do not teach one of the serial bus devices including an ID EPROM connected to the midplane. Baxter teaches a system ID SEEPROM (Serial EEPROM) device located on the backpanel (analogous to the midplane) (See Column 10 Lines 27-29).

One of ordinary skill in the art at the time the invention was made would combine the device of Jobs, Atkinson, Aggarwal, and Simpson, with the devices of Li and Baxter, resulting in the inventions of Claims 15 and 16, in order to provide signals representing the operating parameters of various devices in the computer system such as temperature and voltage (See Column 4 Lines 23-26 and Column 4 Lines 30-33 of Li); and provide a non-volatile way to store important system information (See Column 11 Lines 42-44 of Baxter).

10. Claims 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Atkinson in view of Posner and Buckley.

In reference to Claim 18, Atkinson teaches an application processor (analogous to the local processor) connected to the serial bus through a communication processor (analogous to the bus controller) (See Figure 1 Numbers 9, 12, and 16). Posner teaches a plurality of cross connect switches that can have any number of inputs and outputs (See Figure 11 and Column 1 Lines 38-41); wherein the input (analogous to the first bus portion) is connected to the first switch, the first switch has a connection to the second switch (analogous to the second bus portion), the second switch has a connection to the third switch (analogous to the third bus portion), and the third switch is connected to the output (analogous to the fourth bus portion) (See Figure 11). Buckley teaches a local control logic connected to a valve (analogous to a switch) and controlled by a control processor (See Figure 4, Column 18 Lines 64-67, and Column 19 Lines 1-20) to output signals based on received control signals.

In reference to Claim 19, Atkinson, Posner, and Buckley teach the limitations as in Claim 18 above. Posner teaches that the cross connect switch, under the control of the computer (analogous to the local control logic), can connect a specified input line (analogous to the external circuit board) to a specified output line (See Column 14 Lines 38-40). Since the computer can connect the input line to an output line not connected to the local processor, it inherently connects the external circuit board and the local processor to different portions of the bus.

One of ordinary skill in the art at the time the invention was made would combine the device of Atkinson with the devices of Posner and Buckley, resulting in the inventions of Claims 18 and 19, in order to provide a means of testing the connections between the first portion of the bus and the fourth portion of the bus (See Column 15 Lines 12-19 of Posner); and to reduce the capacitive loading of the devices on the bus by disconnecting segments not in use, since it is known in the art that capacitive loading degrades performance; and to convert the signal compatible with the bus protocol to a signal appropriate for controlling the valve switch (See Column 18 Lines 66-67 and Column 19 Lines 1-6 of Buckley).

11. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Atkinson, Posner, and Buckley as applied to Claim 18 above, and further in view of US Patent Number 5,185,693 to Loftis et al. ("Loftis").

In reference to Claim 22, Atkinson, Posner, and Buckley teach the limitations as in Claim 18 above. Atkinson, Posner, and Buckley do not teach the local control logic

controlling the first, second, and third switches so that if the first switch is disconnected, the second and third switches are controlled by the local processor. Loftis teaches a system of two processors one of which is granted access to a series of I/O devices (analogous to switches 2 and 3) while the other is denied access based on the position of a switch (analogous to switch 1) (See Abstract, Figures 1 and 2, and Column 2 Lines 14-21).

One of ordinary skill in the art at the time the invention was made would combine the device of Atkinson, Posner, and Buckley with the device of Loftis, resulting in the invention of Claim 22, in order to provide redundant control of the bus and switches in the event that the master controller is faulty (See Column 2 Lines 1-4 and Column 2 Lines 7-14 of Loftis).

12. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Atkinson, Posner, and Buckley as applied to Claim 18 above, and further in view of Li.

In reference to Claim 24, Atkinson, Posner, and Buckley teach the limitations as in Claim 18 above. Atkinson, Posner, and Buckley do not teach at least one of a voltage monitor and a temperature sensor are connected to the second portion of the two wire serial bus. Li teaches a serial temperature sensor and a serial voltage sensor (See Figure 2 Number 142 and Column 4 Lines 23-49).

One of ordinary skill in the art at the time the invention was made would combine the device of Atkinson, Posner, and Buckley, with the device of Li, resulting in the inventions of Claim 24, in order to provide signals representing the operating

parameters of various devices connected to the second bus in the computer system such as temperature and voltage (See Column 4 Lines 23-26 and Column 4 Lines 30-33 of Li).

13. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Atkinson, Posner, and Buckley as applied to Claim 18 above, and further in view of Baxter.

In reference to Claim 25, Atkinson, Posner, and Buckley teach the limitations as in Claim 18 above. Atkinson, Posner, and Buckley do not teach an ID EPROM connected to the third portion of the two wire serial bus. Baxter teaches an ID EPROM device (See Figure 2 Number 204).

One of ordinary skill in the art at the time the invention was made would combine the device of Atkinson, Posner, and Buckley with the device of Baxter, resulting in the invention of Claim 25, in order to provide a non-volatile way to store important system information about the devices connected to the third bus portion (See Column 11 Lines 42-44 of Baxter).

14. Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jobs in view of Atkinson and US Patent Number 5,957,985 to Wong et al. ("Wong").

In reference to Claim 1, Jobs teaches a master control processor (See Figure 2 Number 240); a bus controller connected to the processor that implements a serial bus interface between the processor and a plurality of serial bus devices (See Figure 2

Number 202); and a switch configured to electrically connect the circuit board corresponding to the switch to the first circuit board through the serial bus interface when the switch is controlled to be in a first state and to electrically isolate the circuit board corresponding to the switch from the serial bus interface on the first circuit board when the switch is controlled to be in a second state (See Figure 2 Numbers 206 and 208). Jobs does not teach the processor and bus controller being on a first circuit board; a midplane connected to the bus controller on the first circuit board; a plurality of additional circuit boards connected to the serial bus interface through the midplane; each additional board including one or more of the serial bus devices; local control logic for outputting a signal for controlling the state of the switch; and the local control logic controlling the switch to be in the first state when the switches on each of the other of the plurality of additional circuit boards are in the second state. Atkinson teaches a midplane which has a plurality of cards connected to it (See Figure 1 Number 1, and Column 9 Lines 12-15); a serial message bus connecting the cards across the midplane (See Figure 1 Number 9); and a processor and bus interface on a first circuit board (See Figure 1 Numbers 44, 46, and 48). Wong teaches intelligent components that have a local controller for operating the component (See Figures 1, 3, and 6, Column 3 Lines 58-67, and Column 4 Lines 1-7).

In reference to Claim 2, Jobs, Atkinson, and Wong teach the limitations as applied to Claim 1 above. Jobs further teaches basic input-output routines in NVRAM (analogous to the master control logic) connected to the master control processor to control the gates (See Figure 2 Number 228 and Column 2 Lines 46-49). Wong further

teaches that the local controller is under the control of a master controller (analogous to the master control logic) (See Column 4 Lines 21-31).

One of ordinary skill in the art at the time the invention was made would combine the devices of Jobs, Atkinson, and Wong, resulting in the invention of Claims 1 and 2, in order to provide a means for allowing system expandability (See Column 6 Lines 6-10 of Atkinson); increased flexibility (See Column 6 Lines 11-14 of Atkinson); a dense package (See Column 8 Lines 62-63 of Atkinson); to relieve the master from having to operate each device; to manage data flow from the devices (See Column 4 Lines 25-27 of Wong) and to provide redundant control for a device should its controller fail (See Column 5 Lines 16-26 of Wong).

15. Claims 3 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jobs, Atkinson, and Wong as applied to Claim 2 above, and further in view of Simpson.

In reference to Claim 3, Jobs, Atkinson, and Wong teach the limitations as in Claim 2 above. Jobs, Atkinson, and Wong do not teach a multiplexer connected to the output of the bus controller and dividing the serial bus interface into a plurality of sub-buses, only one of which is connected to the bus controller by the multiplexer at any given time. Simpson teaches the use of a multiplexer to divide a serial channel into a plurality of device groups, only one of which is accessible at a time (See Abstract, Figure 4, Column 1, Lines 66-67, and Column 2, Lines 1-15 of Simpson).

In reference to Claim 6, Jobs, Atkinson, Wong, and Simpson teach the limitations as in Claim 3 above. Jobs, Atkinson, and Wong do not teach one of the sub-buses

being connected to the plurality of additional circuit boards Simpson further teaches that a plurality of stations (analogous to the circuit boards) can be connected to each sub-bus through the communication module (See Figure 2 and Column 3 Lines 60-67).

One of ordinary skill in the art at the time the invention was made would combine the device of Jobs, Atkinson, and Wong with the device of Simpson, resulting in the inventions of Claims 3 and 6, in order to allow virtually limitless expansion of the address space (See Column 2, Lines 58-63 of Simpson).

16. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jobs, Atkinson, Wong, and Simpson as applied to Claim 3 above, and further in view of Li and Baxter.

In reference to Claim 4, Jobs, Atkinson, Wong, and Simpson teach the limitations as in Claim 3 above. Jobs, Atkinson, Wong, and Simpson do not teach the serial bus devices including at least one of a temperature sensor, a voltage monitor, and an ID EPROM. Li teaches a serial temperature sensor and a serial voltage sensor (See Column 4 Lines 23-49 of Li). Baxter teaches an ID EPROM device (See Figure 2 Number 204).

In reference to Claim 5, Jobs, Atkinson, Wong, and Simpson teach the limitations as in Claim 3 above. Jobs, Atkinson, Wong, and Simpson do not teach one of the serial bus devices including an ID EPROM connected to the midplane. Baxter teaches a system ID SEEPROM (Serial EEPROM) device located on the backpanel (analogous to the midplane) (See Column 10 Lines 27-29).

One of ordinary skill in the art at the time the invention was made would combine the device of Jobs, Atkinson, Wong, and Simpson, with the devices of Li and Baxter, resulting in the inventions of Claims 4 and 5, in order to provide signals representing the operating parameters of various devices in the computer system such as temperature and voltage (See Column 4 Lines 23-26 and Column 4 Lines 30-33 of Li); and provide a non-volatile way to store important system information (See Column 11 Lines 42-44 of Baxter).

17. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jobs, Atkinson, and Wong as applied to Claim 1 above, and further in view of Posner.

In reference to Claim 7, Jobs, Atkinson, and Wong teach the limitations as in to Claim 1 above. Jobs, Atkinson, and Wong do not teach a first switch for selectively connecting or disconnecting a first portion of a serial bus, implemented by the serial bus interface from the first circuit board, to a second portion of the serial bus; a second switch for selectively connecting or disconnecting the second portion of the serial bus to a third portion of the serial bus; and a third switch for selectively connecting or disconnecting the third portion of the serial bus to a fourth portion of the serial bus. Posner teaches a plurality of cross connect switches that can have any number of inputs and outputs (See Figure 11 and Column 1 Lines 38-41); wherein the input (analogous to the first bus portion) is connected to the first switch, the first switch has a connection to the second switch (analogous to the second bus portion), the second switch has a connection to the third switch (analogous to the third bus portion), and the

third switch is connected to the output (analogous to the fourth bus portion) (See Figure 11).

In reference to Claim 8, Jobs, Atkinson, Wong, and Posner teach the limitations as in Claim 7 above. Atkinson further teaches an application processor (analogous to the local processor) connected to the serial bus through a communication processor (analogous to the bus controller) (See Figure 1 Numbers 9, 12, and 16). Posner further teaches a computer (analogous to the local control logic) that is used to control the first, second, and third switches (See Figure 11 Number 422 and Column 15 Lines 33-34).

One of ordinary skill in the art at the time the invention was made would combine the device of Jobs, Atkinson, and Wong with the device of Posner, resulting in the invention of Claims 7 and 8, in order to provide a means of testing the connections between the first portion of the bus and the fourth portion of the bus (See Column 15 Lines 12-19 of Posner); and to reduce the capacitive loading of the devices on the bus by disconnecting segments not in use, since it is known in the art that capacitive loading degrades performance.

18. Claims 9, 10, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jobs in view of Atkinson and Aggarwal.

In reference to Claim 9, Jobs teaches a device (analogous to the packet forwarding engine) comprising a first circuit board having a master control processor (See Figure 2 Number 240); and a plurality of switches configured to electrically connect a serial bus to the first circuit board when the switch is controlled to be in a first state

and to electrically isolate the serial bus from the first circuit board when the switch is controlled to be in a second state, wherein the switch of a particular serial bus being in the first state only when the switches for each of the other serial busses are in the second state (See Figure 2 Numbers 206 and 208 and Column 2 Lines 26-39). Jobs does not teach a routing engine for consolidating routing information learned from routing protocols in the network; the packet forwarding engine including a midplane; and a plurality of second circuit boards each having a control processor. Aggarwal teaches a routing engine (See Figures 3 and 4, Column 4, Lines 34-38, and Column 5, Lines 49-66 of Aggarwal). Atkinson teaches a midplane which has a plurality of cards connected to it (See Figure 1 Number 1, and Column 9 Lines 12-15); a serial message bus connecting the cards across the midplane (See Figure 1 Number 9); a processor and bus interface on a first circuit board (See Figure 1 Numbers 44, 46, and 48); and a control processor on each of the second circuit boards (See Figure 1 Number 12).

In reference to Claim 10, Jobs, Atkinson, and Aggarwal teach the limitations as in Claim 9 above. Aggarwal further teaches that the network device is a network router (See Figures 3 and 4, Column 2 Lines 26-42, and Column 5, Lines 49-66).

In reference to Claim 13, Jobs, Atkinson, and Aggarwal teach the limitations as applied to Claim 9 above. Jobs further teaches a bus controller connected to the processor that implements a serial bus interface between the processor and a plurality of serial bus devices (See Figure 2 Number 202).

One of ordinary skill in the art at the time the invention was made would combine the devices of Jobs, Atkinson, and Aggarwal, resulting in the invention of Claims 9, 10,

and 13, in order to provide a means for allowing system expandability (See Column 6 Lines 6-10 of Atkinson); increased flexibility (See Column 6 Lines 11-14 of Atkinson); a dense package (See Column 8 Lines 62-63 of Atkinson); and to create a forwarding table allowing the device to determine the proper output port based on the destination address of incoming packets (See Column 6 Lines 4-48 of Aggarwal).

19. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jobs, Atkinson, and Aggarwal as applied to Claim 9 above, and further in view of Wong.

In reference to Claim 11, Jobs, Atkinson, and Aggarwal teach the limitations as in Claim 9 above. Jobs, Atkinson, and Aggarwal do not teach local control logic coupled to receive control information from the master control processor and the control processor corresponding to the second circuit board of the local control logic; and the local control logic controlling the switch to be in the first or second state based on the received control information. Wong teaches intelligent components that have a local controller for operating the component (See Figures 1, 3, and 6, Column 3 Lines 58-67, and Column 4 Lines 1-7) and wherein the component can be controlled by either a master controller or local controller (See Column 4 Lines 21-31).

In reference to Claim 12, Jobs, Atkinson, Aggarwal, and Wong teach the limitations as applied to Claim 11 above. Jobs further teaches basic input-output routines in NVRAM (analogous to the master control logic) connected to the master control processor to control the gates (See Figure 2 Number 228 and Column 2 Lines

46-49). Wong further teaches that the local controller is under the control of a master controller (analogous to the master control logic) (See Column 4 Lines 21-31).

One of ordinary skill in the art at the time the invention was made would combine the device of Jobs, Atkinson, and Aggarwal with the device of Wong, resulting in the invention of Claims 11 and 12, in order to relieve the master from having to operate each device; to manage data flow from the devices (See Column 4 Lines 25-27 of Wong); and to provide redundant control for a device should its controller fail (See Column 5 Lines 16-26 of Wong).

20. Claims 14 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jobs, Atkinson, and Aggarwal as applied to Claim 13 above, and further in view of Simpson.

In reference to Claim 14, Jobs, Atkinson, and Aggarwal teach the limitations as in Claim 13 above. Jobs, Atkinson, and Aggarwal do not teach a multiplexer connected to the output of the bus controller and dividing the serial bus interface into a plurality of sub-buses, only one of which is connected to the bus controller by the multiplexer at any given time. Simpson teaches the use of a multiplexer to divide a serial channel into a plurality of device groups, only one of which is accessible at a time (See Abstract, Figure 4, Column 1, Lines 66-67, and Column 2, Lines 1-15 of Simpson).

In reference to Claim 17, Jobs, Atkinson, Aggarwal, and Simpson teach the limits as applied to Claim 14 above. Atkinson further teaches a serial bus that is connected to a plurality of circuit boards (See Figure 1 Number 9).

One of ordinary skill in the art at the time the invention was made would combine the device of Jobs, Atkinson, and Aggarwal with the device of Simpson, resulting in the inventions of Claims 14 and 17, in order to allow virtually limitless expansion of the address space (See Column 2, Lines 58-63 of Simpson).

21. Claims 15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jobs, Atkinson, Aggarwal, and Simpson as applied to Claim 14 above, and further in view of Li and Baxter.

In reference to Claim 15, Jobs, Atkinson, Aggarwal, and Simpson teach the limitations as in Claim 14 above. Jobs, Atkinson, Aggarwal, and Simpson do not teach the serial bus devices including at least one of a temperature sensor, a voltage monitor, and an ID EPROM. Li teaches a serial temperature sensor and a serial voltage sensor (See Column 4 Lines 23-49 of Li). Baxter teaches an ID EPROM device (See Figure 2 Number 204).

In reference to Claim 16, Jobs, Atkinson, Aggarwal, and Simpson teach the limitations as in Claim 14 above. Jobs, Atkinson, Aggarwal, and Simpson do not teach one of the serial bus devices including an ID EPROM connected to the midplane. Baxter teaches a system ID SEEPROM (Serial EEPROM) device located on the backpanel (analogous to the midplane) (See Column 10 Lines 27-29).

One of ordinary skill in the art at the time the invention was made would combine the device of Jobs, Atkinson, Aggarwal, and Simpson, with the devices of Li and Baxter, resulting in the inventions of Claims 15 and 16, in order to provide signals representing

the operating parameters of various devices in the computer system such as temperature and voltage (See Column 4 Lines 23-26 and Column 4 Lines 30-33 of Li); and provide a non-volatile way to store important system information (See Column 11 Lines 42-44 of Baxter).

22. Claims 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Atkinson in view of Posner and Wong.

In reference to Claim 18, Atkinson teaches an application processor (analogous to the local processor) connected to the serial bus through a communication processor (analogous to the bus controller) (See Figure 1 Numbers 9, 12, and 16). Posner teaches a plurality of cross connect switches that can have any number of inputs and outputs (See Figure 11 and Column 1 Lines 38-41); wherein the input (analogous to the first bus portion) is connected to the first switch, the first switch has a connection to the second switch (analogous to the second bus portion), the second switch has a connection to the third switch (analogous to the third bus portion), and the third switch is connected to the output (analogous to the fourth bus portion) (See Figure 11). Wong teaches intelligent components that have a local controller for operating the component (See Figures 1, 3, and 6, Column 3 Lines 58-67, and Column 4 Lines 1-7) that can receive signals from the master controller (analogous to the external circuit board) and the sensor (analogous to the local processor) (See Figure 3 and Column 6 Lines 26-29).

In reference to Claim 19, Atkinson, Posner, and Wong teach the limitations as in Claim 18 above. Posner further teaches that the cross connect switch, under the

control of the computer (analogous to the local control logic), can connect a specified input line (analogous to the external circuit board) to a specified output line (See Column 14 Lines 38-40). Since the computer can connect the input line to an output line not connected to the local processor, it inherently connects the external circuit board and the local processor to different portions of the bus.

One of ordinary skill in the art at the time the invention was made would combine the device of Atkinson with the devices of Posner and Buckley, resulting in the inventions of Claims 18 and 19, in order to provide a means of testing the connections between the first portion of the bus and the fourth portion of the bus (See Column 15 Lines 12-19 of Posner); to reduce the capacitive loading of the devices on the bus by disconnecting segments not in use, since it is known in the art that capacitive loading degrades performance; to relieve the master from having to operate each device; to manage data flow from the devices (See Column 4 Lines 25-27 of Wong); and to provide redundant control for a device should its controller fail (See Column 5 Lines 16-26 of Wong).

23. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Atkinson, Posner, and Wong as applied to Claim 18 above, and further in view of Loftis.

In reference to Claim 22, Atkinson, Posner, and Wong teach the limitations as in Claim 18 above. Atkinson, Posner, and Wong do not teach the local control logic controlling the first, second, and third switches so that if the first switch is disconnected, the second and third switches are controlled by the local processor. Loftis teaches a

system of two processors one of which is granted access to a series of I/O devices (analogous to switches 2 and 3) while the other is denied access based on the position of a switch (analogous to switch 1) (See Abstract, Figures 1 and 2, and Column 2 Lines 14-21).

One of ordinary skill in the art at the time the invention was made would combine the device of Atkinson, Posner, and Wong with the device of Loftis, resulting in the invention of Claim 22, in order to provide redundant control of the bus and switches in the event that the master controller is faulty (See Column 2 Lines 1-4 and Column 2 Lines 7-14 of Loftis).

24. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Atkinson, Posner, and Wong as applied to Claim 18 above, and further in view of Li.

In reference to Claim 24, Atkinson, Posner, and Wong teach the limitations as in Claim 18 above. Atkinson, Posner, and Wong do not teach at least one of a voltage monitor and a temperature sensor are connected to the second portion of the two wire serial bus. Li teaches a serial temperature sensor and a serial voltage sensor (See Figure 2 Number 142 and Column 4 Lines 23-49).

One of ordinary skill in the art at the time the invention was made would combine the device of Atkinson, Posner, and Wong, with the device of Li, resulting in the inventions of Claim 24, in order to provide signals representing the operating parameters of various devices connected to the second bus in the computer system

such as temperature and voltage (See Column 4 Lines 23-26 and Column 4 Lines 30-33 of Li).

25. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Atkinson, Posner, and Wong as applied to Claim 18 above, and further in view of Baxter.

In reference to Claim 25, Atkinson, Posner, and Wong teach the limitations as in Claim 18 above. Atkinson, Posner, and Wong do not teach an ID EPROM connected to the third portion of the two wire serial bus. Baxter teaches an ID EPROM device (See Figure 2 Number 204).

One of ordinary skill in the art at the time the invention was made would combine the device of Atkinson, Posner, and Wong with the device of Baxter, resulting in the invention of Claim 25, in order to provide a non-volatile way to store important system information about the devices connected to the third bus portion (See Column 11 Lines 42-44 of Baxter).

Allowable Subject Matter

26. Claims 20 and 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

27. Applicant's arguments filed 21 October 2003 in reference to Claims 1-6 have been fully considered but they are not persuasive.

In response to applicant's argument that there is no suggestion to combine the references, the Examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the valve controlled by the local controller of Buckley is analogous to a switch. One of ordinary skill in the art at the time the invention was made would combine the devices of Jobs, Atkinson, and Buckley, resulting in the invention of Claims 1 and 2, in order to provide a means for allowing system expandability (See Column 6 Lines 6-10 of Atkinson); increased flexibility (See Column 6 Lines 11-14 of Atkinson); a dense package (See Column 8 Lines 62-63 of Atkinson); and to convert the signal compatible with the bus protocol to a signal appropriate for controlling the valve switch (See Column 18 Lines 66-67 and Column 19 Lines 1-6 of Buckley). Atkinson teaches an application processor (analogous to the local processor) connected to the serial bus through a communication processor (analogous to the bus controller) (See Figure 1 Numbers 9, 12, and 16).

28. Applicant's arguments, see Page 15 Paragraph 2 through Page 16 Paragraph 2, filed 21 October 2003, with respect to the rejection(s)of claim(s) 7 and 8 under 35 USC § 103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of newly found prior art.

29. Applicant's arguments, see Page 17 Paragraph 1 through Page 18 Paragraph 2, filed 21 October 2003, with respect to the rejection(s)of claim(s) 9-17 under 35 USC § 103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of newly found prior art.

30. Applicant's arguments, see Page 18 Paragraph 3 through Page 21 Paragraph 1, filed 21 October 2003, with respect to the rejection(s)of claim(s) 18, 19, and 24 under 35 USC § 103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of newly found prior art.

31. Applicant's arguments, see Page 21 Paragraph 2, filed 21 October 2003, with respect to the rejection(s)of claim(s) 22 under 35 USC § 103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon

further consideration, a new ground(s) of rejection is made in view of newly found prior art.

32. Applicant's arguments, see Page 21 Paragraph 3, filed 21 October 2003, with respect to the rejection(s)of claim(s) 25 under 35 USC § 103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of newly found prior art.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Cleary whose telephone number is 703-305-5824. The examiner can normally be reached on Monday-Thursday (8-5:30), Alt. Fridays (8-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-5631.

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